Claim Amendments

Applicant has amended claims 1, 4-7, 12, 15, 17-18 and 21-22 and has cancelled claims 2-3 and 13-14 without prejudice. Applicant sets forth below a complete listing of the claims with the corresponding status indicated for each claim.

1. (Currently Amended) A method of increasing resolution of an image-forming device, ~~comprising~~ the ~~steps of~~ method comprising:

applying a sixteen-bit signal representing at least a portion of a source image to a ~~data selecting means~~ multiplexer having sixteen data inputs, so that each bit of the signal corresponds to an input to the ~~data selecting means~~ multiplexer;

at each of a rising and falling edge of a clock pulse, selecting a data input~~,~~ ~~wherein each of the inputs is selected~~ by:

incrementing a counter for each clock cycle;

at each clock cycle, concatenating a binary value of the counter with a value of an inverted clock signal in bitwise fashion to form a data selector code;

inputting the data selector code to the multiplexer; and

selecting a data input corresponding to the data selector code, wherein each input is serially and sequentially selected;

inputting the data bit corresponding to the selected data input to the ~~data selecting means~~ multiplexer; and

transmitting the data bit to a light-emitting element, so that 2 bits are output to the light-emitting element for each clock cycle;

wherein the output specifies any of a width of ~~and~~ or an interval between light pulses emitted by said light-emitting element.

2-3. (Cancelled)

4. (Currently Amended) The method of Claim ~~3~~ 1, wherein the binary value of the counter comprises the three most significant bits of the data selector code and the value of the inverted clock signal comprises the least significant bit.

5. (Currently Amended) The method of Claim ~~4~~ 1, wherein the value of the inverted clock signal is either 0 or 1, 0 corresponding to a low level and 1 corresponding to a high level.

6. (Currently Amended) The method of Claim ~~4~~ 1, wherein sixteen 4-bit data selector codes are generated.

7. (Currently Amended) The method of Claim ~~3~~ 1, wherein said step of selecting a data input further comprises ~~the step of~~: resetting the counter after every eight clock cycles.

8. (Original) The method of Claim 1, wherein the image-forming device comprises a laser printer and wherein the light-emitting device comprises a laser.

9. (Original) The method of Claim 1, wherein the portion of the source image comprises a pixel, and wherein a pixel is specified by a 16-bit value.

10. (Original) The method of Claim 1, said method implemented in a circuit comprising discrete components.

11. (Original) The method of Claim 1, said method implemented in a programmable logic device (PLD).

12. (Currently Amended) A system for increasing resolution of an image-forming device, the system comprising:

~~data selecting means having a plurality of inputs~~ a multiplexer having sixteen data inputs and at least one output, each input corresponding to one bit of a sixteen bit signal applied to the ~~data selecting means~~ multiplexer, the signal representing at least a portion of a source image;

a clock signal; and

means for selecting a data input at each of a rising and falling edge of the clock signal, the means for selecting comprising:

a counter, wherein the counter is incremented for each clock cycle; and

a data selector code comprising the binary value of the counter concatenated with a value of an inverted clock signal in bitwise fashion;

wherein the data selector code is input to the multiplexer, and the data input corresponding to the data selector code is selected, wherein each input is selected in serial and sequential fashion; and

wherein each of the inputs is selected and the corresponding bit input to the ~~data-selecting means~~ multiplexer so that 2 bits are output to a light-emitting element of the image-forming device for each clock cycle, the output specifying any of a width of ~~and intervals~~ or interval between pulses emitted by said light-emitting element.

13-14. (Cancelled)

15. (Currently Amended) The system of Claim ~~14~~ 12, wherein the binary value of the counter comprises the three most significant bits of the data selector code and the value of the inverted clock signal comprises the least significant bit.

16. (Original) The system of Claim 15, wherein the value of the inverted clock signal is either 0 or 1, 0 corresponding to a low level and 1 corresponding to a high level.

17. (Currently Amended) The system of Claim ~~14~~ 12, wherein sixteen 4-bit data selector codes are generated.

18. (Currently Amended) The system of Claim ~~14~~ 12, wherein the counter is reset after every eight clock cycles.

19. (Original) The system of Claim 12, wherein the image-forming device comprises a laser printer and wherein the light-emitting device comprises a laser.

20. (Original) The system of Claim 12, wherein the portion of the source image comprises a pixel, and wherein 16 bits represent a pixel.

21. (Currently Amended) The system of Claim 12, the system comprising a circuit composed of discrete components.

22. (Currently Amended) The system of Claim ~~1~~ 12, the system comprising a programmable logic device (PLD).